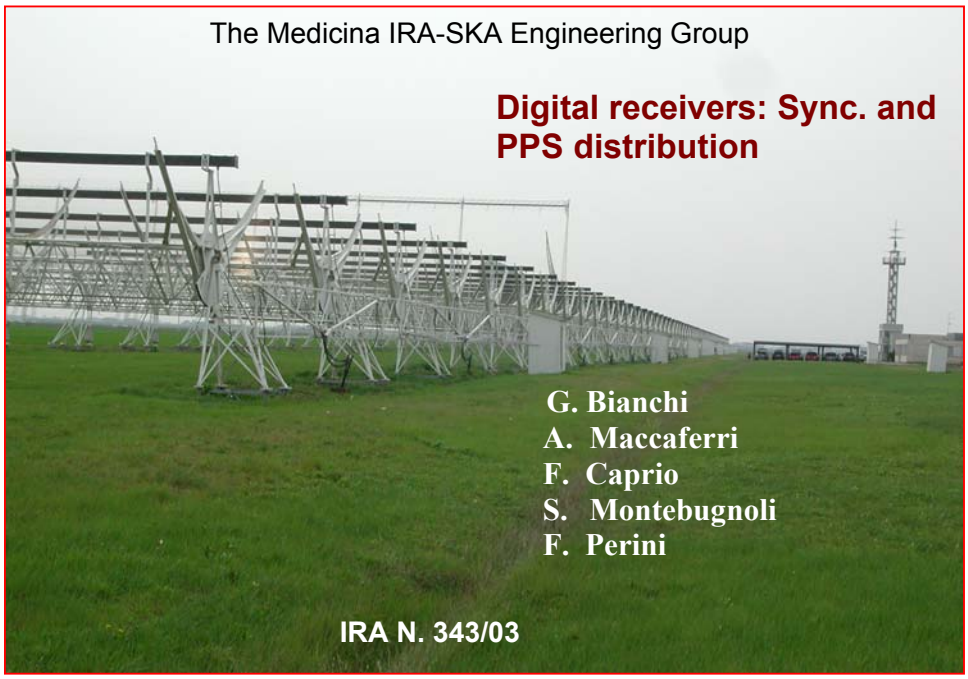
The Medicina IRA-SKA Engineering Group

Digital receivers: Sync. and PPS distribution



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IRA N. 343/03

Abstract

The Northern Cross (Medicina, Bologna - Italy) is a large array (30.000 m^2) suitable to be transformed in a very interesting test bed aimed to gain experiences to be flown in the Square Kilometre Array (SKA) concepts definition and construction. Several substantial modifications have to be introduced in the existing array and many new blocks need to be designed during this activity. First results of a low cost and low jitter optical link (about 800 mt) for sync. and Pulse Per Second (PPS) distribution are reported in this paper.

Introduction

The aim is to send both clock and PPS (Pulse Per Second) signals from the processing room to the digital receivers, installed outside close to the antenna, via an optical link. This operation is critical in this application because a minimum difference in the rising time of the clock signals would means to sample different wavefront. In the beamforming phase this could mean to sum together non coherent signals. The board has two different optical fibers: one for the clock and the other one for the PPS signals. We will report the results of tests performed on a first prototype board.

Prototype implementation

The board for the sync distribution is designed to operate within the new system for data transmission, from the Northern Cross antenna to the processing room. The whole chain is shown in fig.1. The sync signals (clock and PPS) are request to synchronize all digital devices, as the ADCs (Analog to Digital Converter) and DDCs (Digital Down Converter), at the sampling frequency of 80MHz (5MHz bandwidth centered at 30MHz IF value). The same sync signal is sent to DDCs, devoted to down convert the sampled IF to the base band. In order to completely synchronize the digital receiver a PPS is sent.
We realized the prototype using low cost commercial devices, probably able to satisfy the SKA specifications. We concentrated our design on the long distances opto-electronic devices. It has been chosen the usage of an optical fiber link instead of a copper one, because of the well known advantages of the optical links. These can transport a signal through long distance cables with a high bit rate, high electrical isolation (between processing room and antenna) and little thermal excursion influence. At the beginning, we tried to design a board with a Manchester encoder, but we found no commercial devices able to work at 80MHz. In the first prototype board, both signal (clock and PPS) were sent by the Agilent transceiver HFBR-5805A, but first tests gave bad results for low bit rate transmission of the PPS signal. In the second solution a different link for the PPS, an Agilent transmitter (HFBR-1312) and a receiver (HFBR-2316) with a custom driver and receiver circuits respectively, was used. The main difference between the above reported links is the coupling: the first was AC and the second DC coupled.

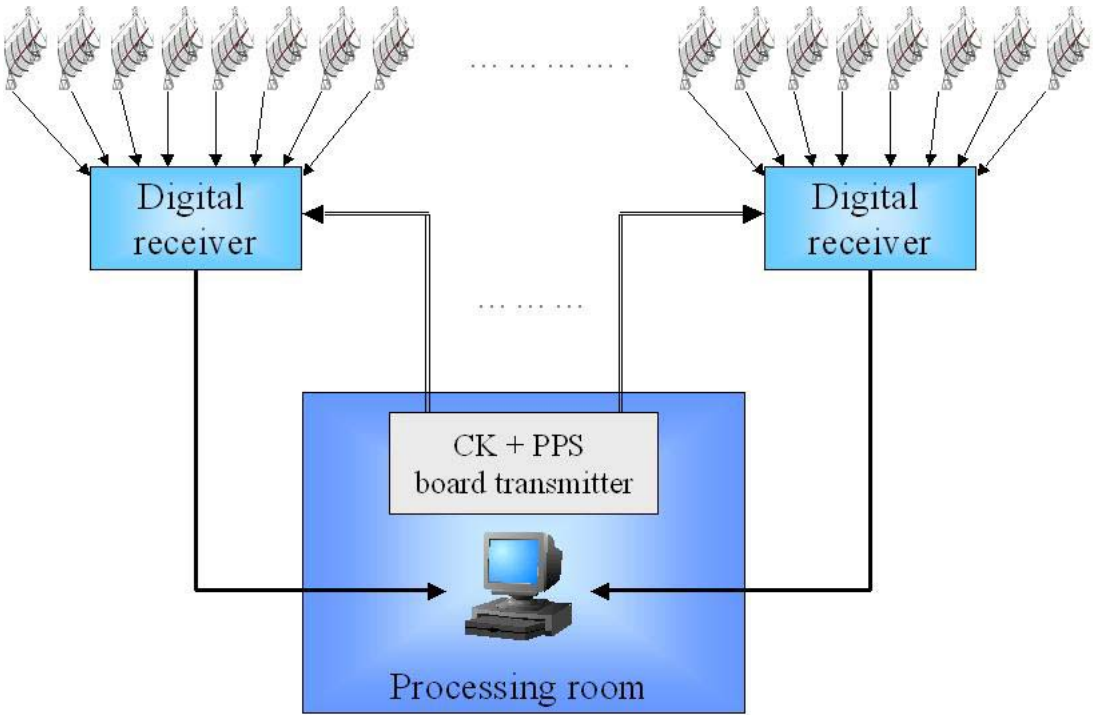

Fig. 1: Clock and PPS distribution.

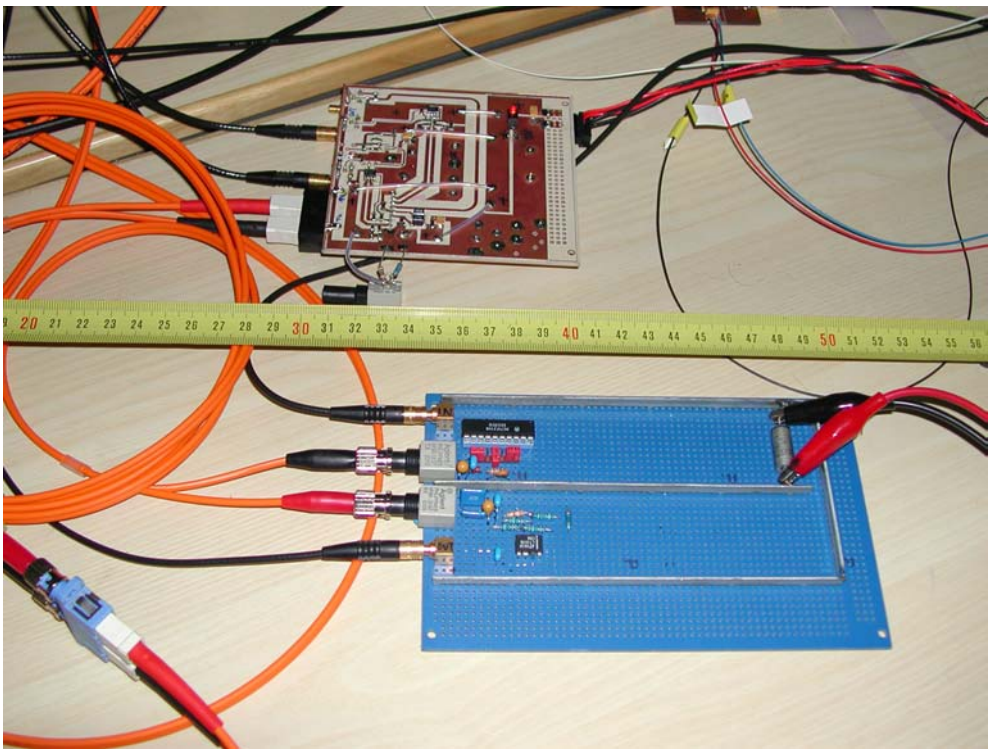

Fig. 2: Clock and PPS test boards

The test board is shown in fig. 2, while its block diagram is reported in fig. 3. The circuit can accept two different inputs, one 80MHz sine-wave and the second 80MHz square-wave; for testing the board, we took signal in output at the squarer (worst case). Tests have been performed exploiting the transceiver present on the board using the output connected with a single 600m long fiber to the input. In the board final version, the transceiver will still work in both directions. The TX will be used to send the clock and the RX will be used to control the correctness of the signal transmission. The PPS board is designed and tested following the same philosophy.
In fig. 4 the instrumentation test set up is reported. We connected the PPS signal with the signal generator, so we were sure that the signals were synchronous at the input of the test board.

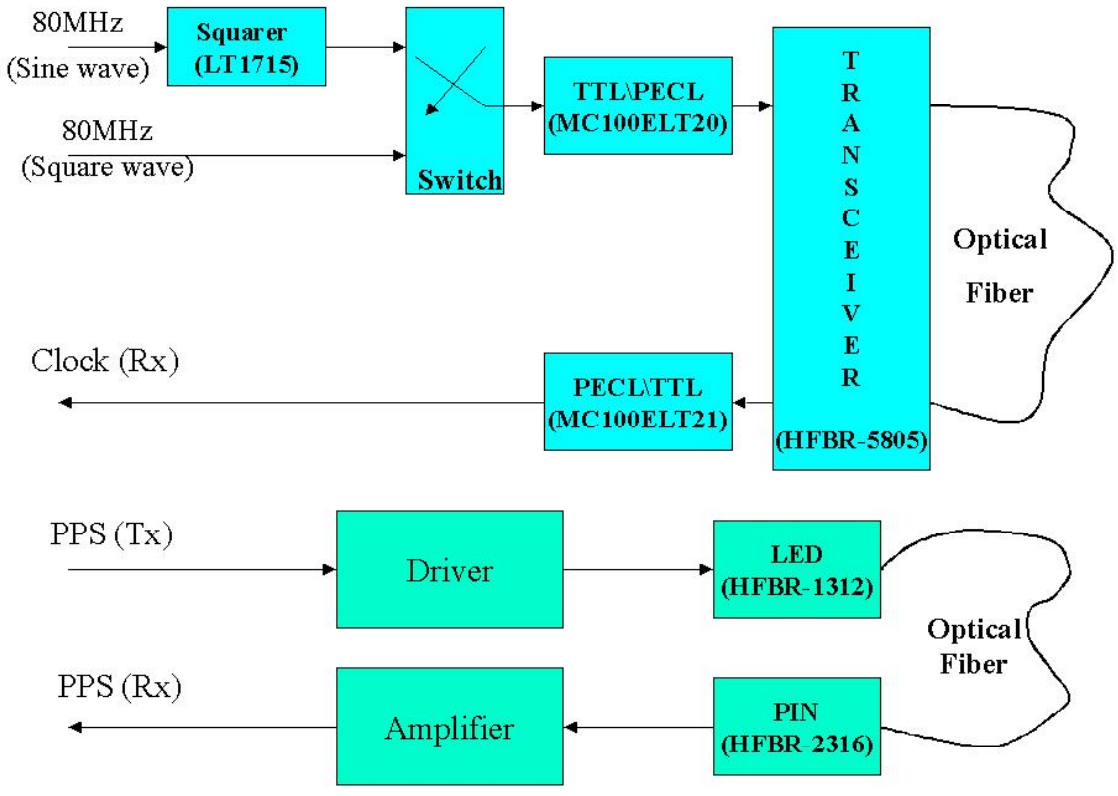

Fig. 3: CK and PPS block diagrams.

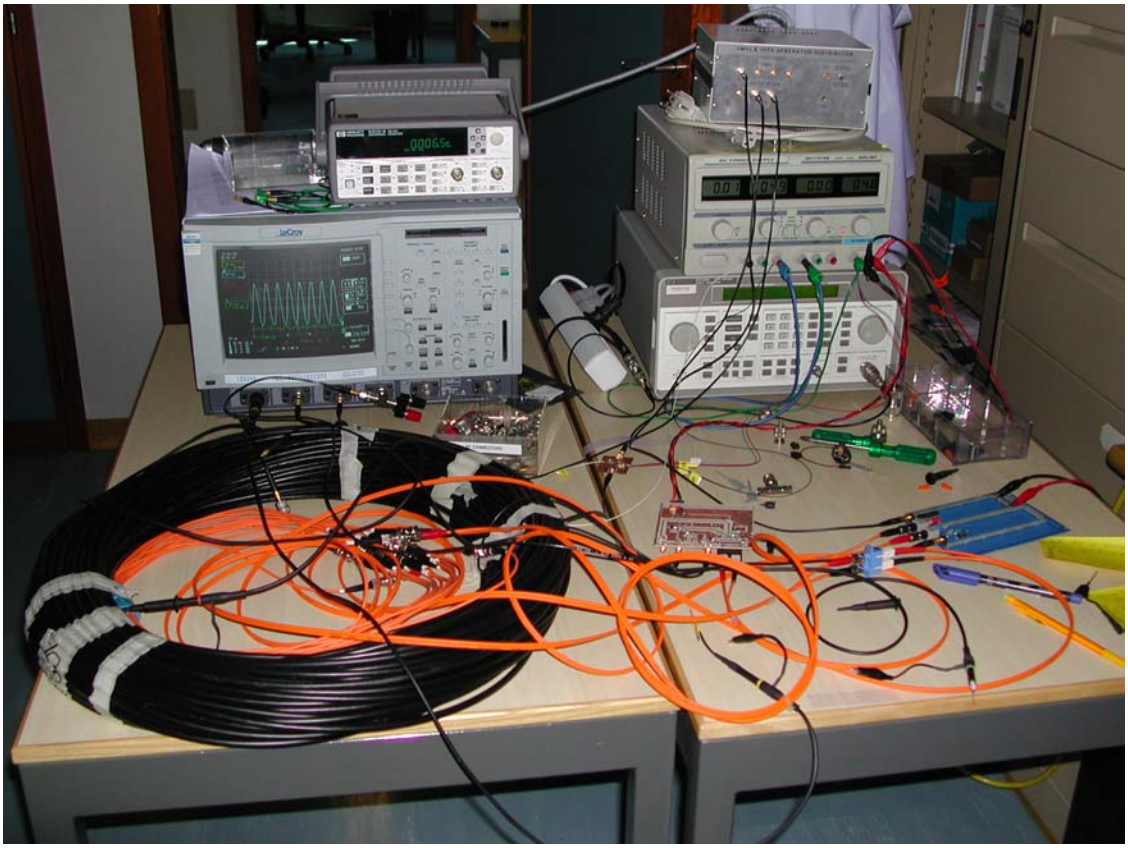

Fig. 4: PPS and Clock test set up.

Results

Results are shown in fig. 5, where the traces visualized by the oscilloscope are drawn after having acquired the board output signals for 6 hours. These traces represent the clock (blue trace) and the PPS (red trace). The traces are formed by several signals overlapped during 6 hours acquisition. It is important to note the variation of the signals, it seems to be less than 500 psec. This test has been performed with a 600m fiber link between the output and input of the RTX board, which has introduced a delay (3 μsec) show in green at the bottom of the fig.5. This delay is referred to the PPS signal at the input of the board, being the trigger signal used by the oscilloscope as sync reference signal. These results are obtained at room temperature, but a test at extended temperature range is planned.

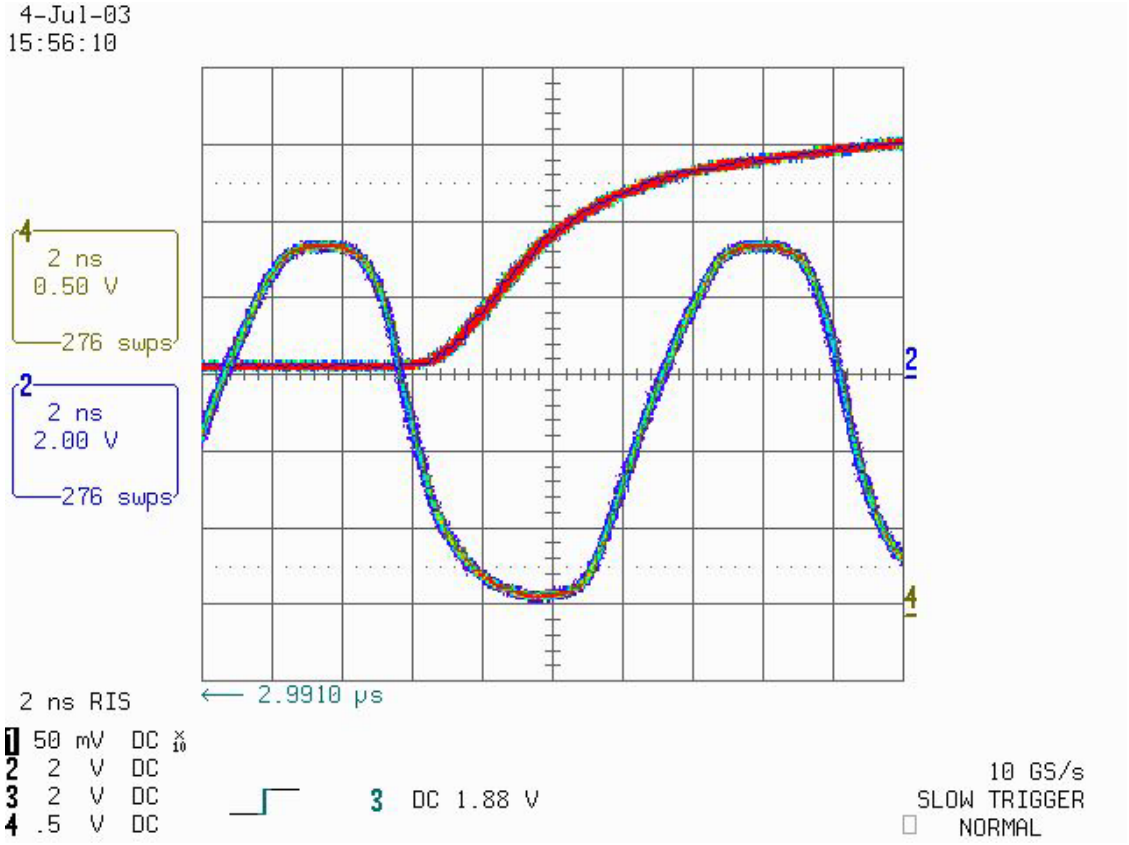

Fig. 5: Clock and PPS output signals after 6 hours of acquisition.

Conclusions

Results shown in figure 5, represent the sum of several signals acquired for 6 hours. The signals jitter is so narrow (less than 500 psec, measured in specific window of the oscilloscope) that we can consider the board reliable for our specifications (target is to have the lowest phase delay, 4% in this case). The whole sync system will be composed by 28 links (14 for the clock and 14 for the PPS signals) connected to the 14 cabins. Every cabin will receive one couple of signals (clock+PPS) for every digital receiver (64 in final configuration) housed in that cabin. We plan to install fibers with the same length in order to have the same delay. An alternative could be the installation of fibers with different length and later compensation of the delay differences.

Appendix:

The ICS570 chip: an extremely low jitter PLL clock multiplier

The clock at the input of the digital receivers, needs to present an extremely low jitter. In standard application, the sync is generated by synthesizer clocked with a reference signal

from a station H-Maser (5/10 MHz). In this note we present a PLL clock multiplier chip (80 MHz out with a 5 MHz reference) that potentially could replace a much more expensive synthesizer. A test board based on the ICS570 PLL clock multiplier chip, has been designed and tested (figure 6). Very promising results has been obtained as visible in figure 7. The output signal shows a 300 psec jitter (blue trace) after 2 hours of acquisition.

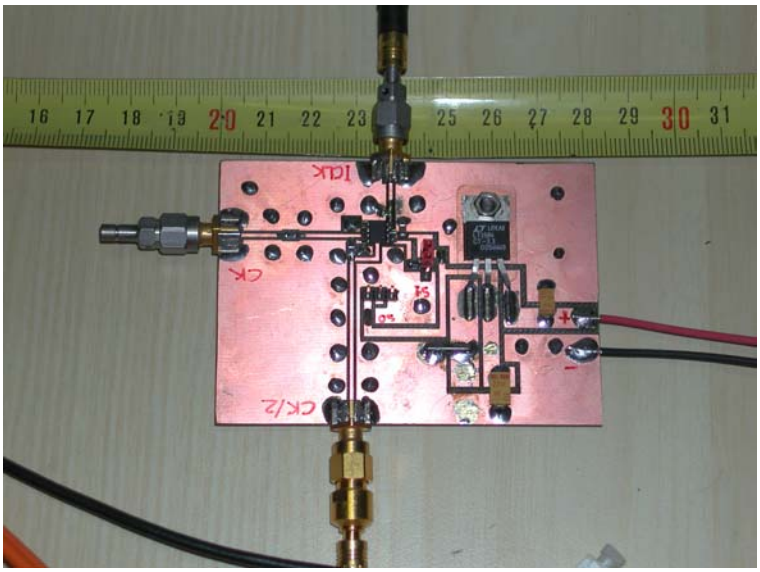

Fig. 6: PLL clock multiplier test boards.

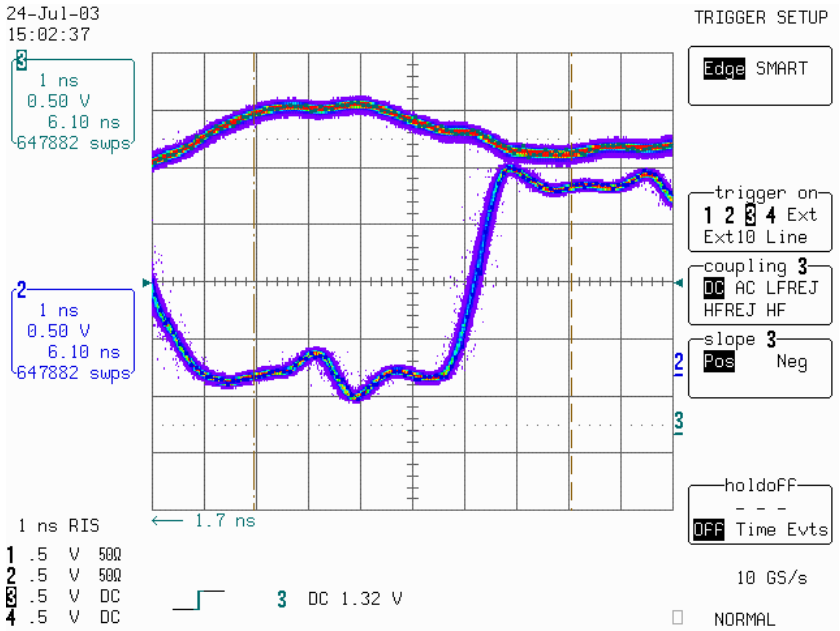

Fig. 7: 80MHz PLL clock multiplier output after 2 hours of acquisition.

As a test, the 80MHz PLL output has been sent to the optical clock link. Results are shown in figure 8. After 3 hours of acquisition, the measured jitter is less than 800 psec. In conclusion, using the PLL multiplier ICS570, the jitter is worsened of about 300psec.

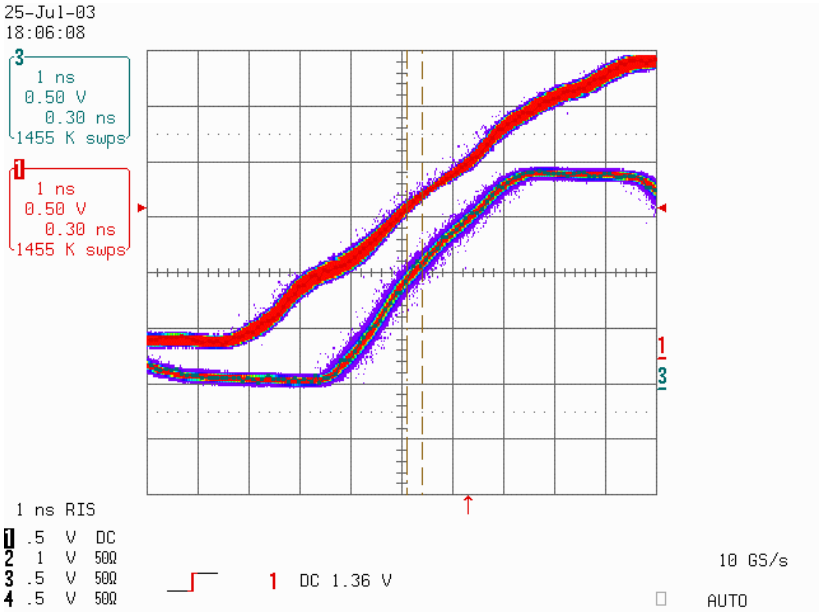

Fig. 8: 80MHz optical link output (blue trace). Red color trace represents the 5MHz reference. Time acquisition: 3 hours.

In figure 9 a snapshot acquisition of the 5MHz input clock (blue trace), the ICS570 PLL clock multiplier output signal (red) and the 80MHz clock at the optical link output (green), is reported.

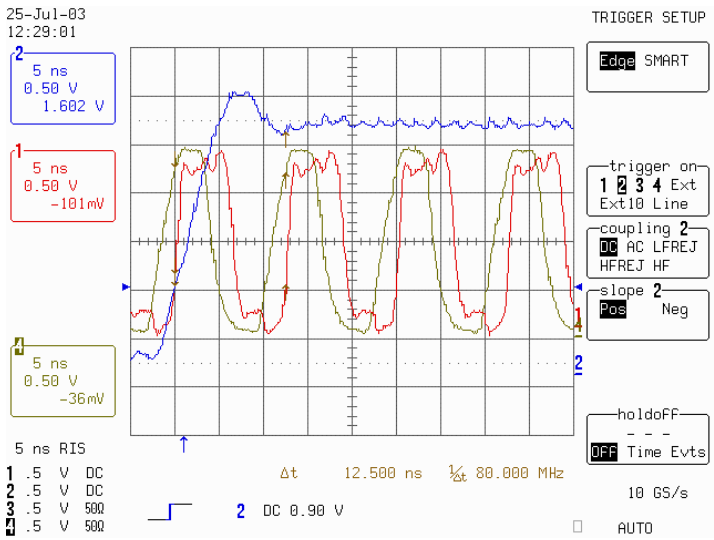

Fig. 9: Snapshot acquisition of the 5MHz input, 80MHz PLL output and optical link 80MHz output.